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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,965	07/08/2003	Janko Boehm	DE920010007US1	8863

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,965	BOEHM ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8,9 and 58-93* is/are pending in the application.

4a) Of the above claim(s) *58-93* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Election/Restrictions

1. Newly submitted claims 58-93 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: applicant claims a method, computer program product and system such that an I/O device value determines/selects the communication protocol a configurable controller chip will meet. The original claims, while supporting a plurality of I/O protocols, e.g., claims 6 and 7, does not specifically state adapting the controller chip to the communication protocol based on the I/O device value that exists on the I/O device. The original claims merely suggest the adaptation of the controller to what the I/O device needs, e.g., assigning I/O pins according to the needs of each I/O device per claim 9, but this can easily be construed to be adapting the I/O pins for more data throughput, special conditions specific to the I/O device outside of the defined protocol, etc., essentially considerations that are not related to the communication protocol.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 58-93 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Response to Arguments

2. Applicant's arguments filed 07/08/2005 have been fully considered but they are not persuasive.

3. Applicant contends Rangasayee does not disclose assigning "a special number and type of interfaces to each I/O device" and "I/O pins according to the needs of the I/O device", further arguing that Rangasayee only has uniform ports and fixed I/O pins per port.

Examiner disagrees based on the broad recitation these particular limitations in the claim language. Under the broadest reasonable interpretation of the claims, one of ordinary skill in the art would construe a "special number and type of interfaces" simply anything that meets the desired application that the programmable logic array is applied to. The CPLD IC, shown in Fig. 11, is by definition "special" since it is programmable to suite the need of the application, e.g., whatever device(s) it is attached to. For instance in Fig. 11, any one of the pins can programmed to connect to any one of the other pins by way of a virtual circuit shown in bold (virtual circuit creation disclosed in Column 10, lines 33-65; Column 12). Not all of the pins need to be utilized, only what is necessary to suit the application, further showing that a special *number* of pins (i.e., 514 and 516) and interfaces (i.e., the virtual circuit making up the connection) is achieved. One of ordinary skill in the art will know that some of the pins may not be used since the I/O devices may not require the use of all the pins.

4. Applicant contends Rangasayee does not disclose the initialization of the I/O devices, stated as obvious in item 4 of the previous Office Action.

Examiner maintains his rejection that the initializing of the I/O devices would be obvious to one of ordinary skill in the art at the time of Rangasayee's invention. First, the I/O devices from the broad recitations can be anything that performs input output. Nowhere does claim 1 define or limit what an I/O device is. Per Rangasayee, I/O devices can comprise devices coupled to the pins 514 and 516, external *or internal* to the chip. Thus, the programmable switch unit,

element 506 of Fig. 11, can be construed to be I/O devices, inputting a signal from one pin and outputting the signal to another pin. Secondly, as stated in the previous office action, the CPLD must be initialized before it can be used which requires programming instructions by an external source. The applicant desired adequate evidence, and thus the Examiner brings in reference 6,507,213 to Dangat which discloses that CPLDs must be initialized every time the CPLD is turned on or reprogrammed (Column 1, lines 29-67, particularly noting that the arrangement and operation of components inside a CPLD is programmed by instructions from nonvolatile memory, this programming is implemented every time the CPLD is turned on or configured, Column 1, lines 44-47). To the Examiner's knowledge, this is something that is standard and well-known to one of ordinary skill in the art and the applicant is welcomed to provide evidence that shows otherwise. Thus, during the initialization of the CPLD, the I/O devices represented by programming switch units (Fig. 11, element 506) are initialized, causing the assignment of particular interfaces and pins.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 8 and 9 stand rejected under 35 USC 103(a) as being unpatentable over US Pat. No. 6,181,159 to Rangasayee.

7. Per Claim 1, Rangasayee discloses a method, computer system and program product for controlling a plurality of I/O devices (Fig. 11, elements 514 and 516 being multiple I/O ports

attached to I/O devices 506) being attached to a microprocessor by (Column 9, lines 5-12, microprocessor can program the programmable device, e.g., element 500 of Fig. 11) a special number and type of interfaces (Fig. 11, chip has special number and type of interface shown by the programming switch unit, the pins, and the virtual circuit that is created depending on what the desired application of the CPLD is) comprising: connecting a configurable chip (Fig. 11, element 500 can be an FPGA or CPLD, Column 1, lines 39-52) to the I/O space of said microprocessor (virtual circuit created programmed by the microprocessor, Column 9, lines 5-13, is accomplished through the I/O pins of the microprocessor, hence through the I/O space of the processor), said configurable chip having a switch matrix (Fig. 2-4, cross bar switch matrix); and assigning to said switch matrix said special number and type of interfaces to each I/O device (programming switch unit 506 is assigned a special number of paths and pins based on application, e.g., the virtual circuit is special for each unit 506 based on what it is programmed).

Rangasayee does not disclose expressly the I/O devices are initialized or the step of performing the assignments of the special number and type of interfaces during initialization.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to initialize the programmable switch units 506 (I/O devices).

The suggestion/motivation for doing so would have been programmable devices, in particularly CPLDs and FPGAs require initial instruction on how to configure the logic blocks and programmable routes on the device prior to ordinary use. This step is always done during initialization where an external source sends configuration data to the programmable device in order to configure the device for the desired functionality as is well known to one of ordinary skill in the art.

Therefore, it would have been obvious to initialize the programmable logic device, which entails initializing the I/O devices, so that the desired routing configuration is established in order to appropriately use the device.

8. Per Claim 8, Rangasayee discloses claim 1, wherein it is further obvious that the internal paths and pins are required to correspond to the correct pins of the I/O devices (506) attached to the CPLD. The designer/routing mechanism of the CPLD must associate pins on the CPLD to I/O devices closest to the pins to minimize latency. For instance, I/O device 506-1 would not associate connect pin 514-5 with 514-4 since the I/O device that can establish that path, e.g., the lower left I/O device 506 in Fig. 11 would handle the path routing due to it's proximity.

9. Per Claim 9, Rangasayee discloses claim 1, further comprising switching the hardware using ID bits on each I/O device (Column 12, 50+, the virtual link (VL) established on the I/O devices 506 on Fig. 6 are programmed by the LB block 502, where the LB block "directing the programmable switch unit to couple selected ones of the I/O lines 520". The LB block must inherently be able to identify the I/O device 506 in order to direct/program the VL, and this identification in digital logic inherently equates to a plurality of bits given that plurality of I/O devices 506 on the chip).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
08/24/2005

KIM HUYNH
PRIMARY EXAMINER
9/05/05